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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,780	02/13/2002	James E. Bader	56162.00362	9493

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EXAMINER	
SORRELL, ERON J	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 07/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,780	BADER ET AL.	
	Examiner	Art Unit	
	Eron J. Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/13/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7,9,10,12-17,19,20,22-27,29,30,32-36, and 38-40 are rejected under 35 U.S.C. 102(e) as being anticipated by Mason (U.S. Patent No. 6,393,547).

3. Referring to method claim 1, Mason a method for sharing a general purpose input/output (GPIO) line of an integrated circuit between at least two circuit components, the method comprising:

providing, using the GPIO line, a first input from a first circuit component to the integrated circuit during a first time (see lines 9-55 of column 4);

providing, using the GPIO line, a first output from the integrated circuit to a second circuit component during a second time (see lines 9-55 of column 4); and

wherein the first circuit component and the second circuit component are concurrently coupled to the GPIO line (see figure 2 and lines 9-55 of column 4).

4. Referring to method claims 2,3,14,15, apparatus claims 24 and 25, system claims 34 and 35, Mason teaches the step of providing the first input includes providing the first input at a low frequency relative to a switching frequency of the GPIO line and wherein the first time is at least in part concurrent with the second time (see paragraph bridging columns 1 and 2, note at lines 43-50 of column 2, Mason teaches configuring the system to account for output devices that can tolerate insignificant periods of output signal loss and the switching frequency of the GPIO pin (line) is dependent on this configuration).

5. Referring to method claims 4 and 16, apparatus claim 26, and system claim 36, Mason teaches the first time is different from the second time (see lines 9-55 of column 4).

6. Referring to claim 5, Mason teaches the step of providing, using the GPIO line, a second input from the first circuit component to the integrated circuit during a third time different from the first time (see lines 43-50 of column 2).

7. Referring to claim 6, Mason teaches the step of providing, using the GPIO line, a second output from the integrated circuit to the second circuit component during a third time different from the second time (see lines 43-50 of column 2).

8. Referring to claim 7, Mason teaches the step of providing a first input comprises the step of configuring the GPIO line as an input line during a portion of the first time, and the step of providing a first output comprises the step of configuring the GPIO line as an output line during the second time (see lines 9-55 of column 2).

9. Referring to method claims 9,10,19, and 20, apparatus claims 29 and 30, system claims 39 and 40, Mason teaches the first circuit component includes a switch (see item labeled 46 in figure 2) and the second circuit component includes an LED (see item labeled 50 in figure 2).

10. Referring to method claims 12 and 22, apparatus claim 32, and system claim 38, Mason teaches the integrated circuit comprises one or more of a group consisting of: a microprocessor, a microcontroller, a field programmable gate array, a programmable logic device, a programmable logic array, and an application specific integrated circuit (see lines 9-15 of column 4, wherein Mason teaches at least a microprocessor).

11. Referring to method claim 13, apparatus claim 23, and system claim 33, Mason teaches a method for sharing a general purpose input/output (GPIO) line of an integrated circuit, the method comprising:

connecting a first component to the GPIO line (see figure 2 and lines 9-55 of column 4);

connecting a second circuit component to the GPIO line concurrently with the first circuit component (see figure 2 and lines 9-55 of column 4);

wherein the first circuit component is to provide input to the integrated circuit using the GPIO line during a first time (see lines 9-55 of column 4); and

wherein the second circuit component is to receive an output from the integrated circuit using the GPIO line during a second time (see lines 9-55 of column 4).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 11,21,31, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mason in view of AAPA.

14. Referring to method claims 11 and 21, apparatus claim 31, and system claim 41, Mason is silent on the second circuit component further comprising an inverter.

The applicant admits on page 1, paragraph 2, that inverters are typically interfaced with GPIO lines and made use of by microcomputer systems.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the method and system of Mason such that the second circuit component further comprises an inverter in order to be used in a wide variety of applications.

15. Claims 8,18,28, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mason in view of The Authoritative Dictionary of IEEE Standards Terms (hereinafter "The IEEE Dictionary").

16. Referring to method claims 8 and 18, apparatus claim 28, system claim 37, Mason fails to explicitly set forth the limitation that the portion of the first time includes a first predetermined sequence of processing cycles and the second time includes a second predetermined sequence of processing cycles different from the first sequence, however, Mason does disclose the microprocessor uses a method of time-sharing the GPIO pin (line), a process known in the art as time division multiplexing.

The IEEE dictionary defines time division multiplexing as a method in which two or more channels of information are transmitted over the same link by allocating a different time interval for the transmission of each channel. This time interval directly correlates to predetermined processing cycles.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system and method of Mason with the above teachings of The IEEE

Dictionary in order to properly transmitted distinct channels of data over the same GPIO line.

17. Claims 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mason in view of Vitenberg (U.S. Patent No. 6,813,343).

18. Referring to claims 42-44, Mason fails to teach the system comprises a modem, wherein the modem comprises the first and second circuit components and also fails to teach the system is a DSL system.

Vitenberg teaches a DSL system comprising a modem, wherein the modem comprises first and second circuit components (see lines 36-54 of column 6).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Mason with the above teachings of Vitenberg in order to reduce the pin count, and subsequently the cost and complexity, in the microprocessor of Vitenberg.

Response to Arguments

19. Applicant's arguments with respect to claims 1-44 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,496,880 to Ma et al. teaches a method and system for sharing a GPIO pin (line).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on 571-272-4083. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJS
July 14, 2005

KIM HUYNH
PRIMARY EXAMINER
7/15/05